

Drawings

The Examiner is respectfully requested to acknowledge on the record the status of the drawings as filed along with the present application, so that any necessary corrections may be timely made.

Claims Rejections-35 U.S.C.102

Claims 1-10, 14, 15 and 21-23 have been rejected under 35 U.S.C. 102(e) as being unpatentable over the Lee et al. reference (U.S. Patent No. 6,136,695). This rejection is respectfully traversed for the following reasons.

With regard to claim 1, the Examiner has alleged on page 2 of the current Office Action dated April 2, 2002, that the Lee et al. reference discloses "forming a conductive line 20, which is to be connected to the conductive region 25, on the first interlayer dielectric layer 60". However, conductive structures 20 are not formed on first dielectric lining 60, as may be readily appreciated in view of Fig. 2C of the Lee et al. reference. Particularly, conductive structures 20 are formed on substrate 10, and first dielectric lining 60 is formed on conductive structure 20 and on contact area 25 between conductive structures 20. Accordingly, the Lee et al. reference as relied upon by the Examiner does not disclose a method of fabricating a semiconductor device including in combination "forming a conductive line, which is to be connected to the conductive region, on the first interlayer dielectric layer", as featured in claim 1. Applicants therefore respectfully submit that the method of fabricating a semiconductor device of

claim 1 distinguishes over the Lee et al. reference as relied upon by the Examiner, and that this rejection of claims 1-8 is improper for at least these reasons.

With further regard to claim 1, the Examiner has alleged on page 3 of the Office Action that the Lee et al. reference discloses "filling the contact hole 55 with a conductive material to connect the conductive line 20 to the conductive region 25". However, conductive structures 20 of the Lee et al. reference are not connected to contact area 25 by a conductive material. For example, contact layer 90 is connected to contact area 25 as illustrated in Fig. 2F, not to conductive structures 20. Accordingly, the Lee et al. reference does not disclose a method of fabricating a semiconductor device including in combination "filling the contact hole with a conductive material to connect the conductive line to the conductive region", as featured in claim 1. Applicants therefore respectfully submit that the method of fabricating a semiconductor device of claim 1 distinguishes over the Lee et al. reference as relied upon by the Examiner, and that this rejection of claims 1-8 is improper for at least these additional reasons.

Applicants also respectfully submit that the method of fabricating semiconductor devices of claim 9 distinguishes over the Lee et al. reference for at least somewhat similar reasons as set forth above with respect to claim 1. Particularly, the Lee et al. reference does not disclose a method of fabricating semiconductor devices including in combination "forming a conductive line, which is to be connected to the conductive region, on the first interlayer dielectric layer, the conductive line having a gap therein of a predetermined width". As emphasized previously, conductive structures 20 of the Lee

et al. reference are formed on substrate 10, and first dielectric lining 60 is formed on conductive structures 20 and on contact area 25 between conductive structures 20. Also, the Lee et al. reference does not disclose a method of fabricating semiconductor devices including in combination "filling the contact hole with a conductive material to connect the conductive line to the conductive region". As emphasized previously, conductive structures 20 of the Lee et al. reference are not connected to contact area 25 by a conductive material. Accordingly, Applicants respectfully submit that the method of fabricating semiconductor devices of claim 9 distinguishes over the Lee et al. reference as relied upon by the Examiner, and that this rejection of claims 9, 10, 14, 15 and 21-23 is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.

A handwritten signature in black ink, appearing to read "A. J. Telesz, Jr.", with a stylized flourish at the end.

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